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E. Willis
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Sion C. QUINLAN and Tim J. BALES Attorney Docket No.: 500986.02

Filed : Concurrently herewith

Title : SEMICONDUCTOR PACKAGE ASSEMBLY AND METHOD FOR ELECTRICALLY ISOLATING MODULES

INFORMATION DISCLOSURE STATEMENT

Box Patent Assignments
Commissioner of Patents
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicants wish to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449 (copies of the cited references are enclosed). Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicants' duty to disclose all information they are aware of which is believed relevant to the examination of the above-identified application, applicants believe that their invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP

Andrew F. Pratt
Registration No. 48,985

Enclosures:
Form PTO-1449; Cited References

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FORM PTO-1449 (REV 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500986.02	APPLICATION NO. Not Yet Assigned
		APPLICANT(S) Sion C. QUINLAN and Tim J. BALES	
		FILING DATE Concurrently herewith	GROUP ART UNIT 2829

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

1625 U.S. PTO 10/057205 01/26/02

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
SBG	AA	5,975,958	11-02-99	Weidler	439	620	
SBG	AB	6,023,202	02-08-00	Hill	333	24	
SBG	AC	6,109,971	08-29-00	Vadlakonda	439	620	
SBG	AD	6,124,756	09-26-00	Yaklin et al.	327	564	
SBG	AE	6,147,542	11-14-00	Yaklin	327	344	
SBG	AF	6,249,171 B1	06-19-01	Yaklin et al.	327	382	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
\	AG							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

SBG	AH	Al-sarawi, Said F., "Wire Bonded Stacked Chips," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node35," January 25, 2002, pp. 1-2
SBG	AI	Al-sarawi, Said F., "Blind Castellation Interconnection," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node44," January 25, 2002, p. 1
SBG	AJ	Al-sarawi, Said F., "Silicon Efficiency," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node20," January 25, 2002, pp. 1-2
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EXAMINER	DATE CONSIDERED
A.D. D	8/21/03

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

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OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*		
SBG	AL	Al-sarawi, Said F., "Noise," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node23," January 25, 2002, p. 1
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SBG	AU	Al-sarawi, Said F., "Folded Flex Circuits," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node34," January 25, 2002, p. 1
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	BD	
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